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				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Katherine L. Saenger et al.
				Art Unit	<del>N/A</del> 2812
				Examiner Name	<del>Not Yet Assigned</del> GEYER
Sheet	1	of	1	Attorney Docket Number	YOR920030530US1 CBLH/20140-00316-US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
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SOB	CA	JAKUB KEDZIERSKI, et al., Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation, IBM Semiconductor Research and Development Center pgs. 247-250	
SOB	CB	B. GUILLAUMOT, et al., 75nm Damascene Metal Gate and High-k Integration for Advanced CMOS Devices, Cedex France, Meylan France, Marseille France, pgs. 355-358	
SOB	CC	KATHERINE L. SAENGER, et al., A Selective Etching Process for Chemically Inert High-k Oxides, Mat. Res. Soc. Symp. Proc. Vol. 745© 2003 Material Research Society, IBM Research Division, T.J. Watson Research Center	
SOB	CD	MATSUO J. YAMADA, et al., Surface processing by gas cluster ion beams at the atomic (molecular) level, Ion Beam Engineering Experimental Laboratory, Kyoto University, Sakyo, Kyoto 606, Japan	

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Examiner Signature	<i>W. G.</i>	Date Considered	6-1-05
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